

# New Era of Panel Based Technology for Packaging, and Potential of Glass

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# CONNECT

# Connecting the World

## Connecting the World



*Smart Mobility*



*Green Energy  
/Environment*



*Smart Factory*

# BIG DATA

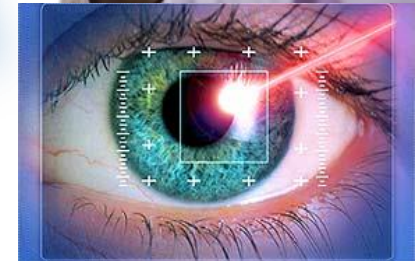
# AI & IOT & SENSORS



*Smart Mobile  
Devices  
Wearable Devices  
Wireless (5G)*



*Medical*



*Security/Biometrics*

## Glass and Electronics

Designing  
/Decorative  
material

Opening  
material

Laboratory  
glass

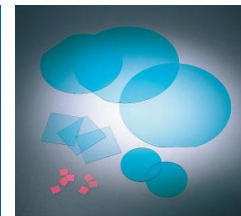
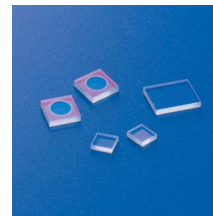
Display  
devices

Optical  
component

Human  
interface  
devices

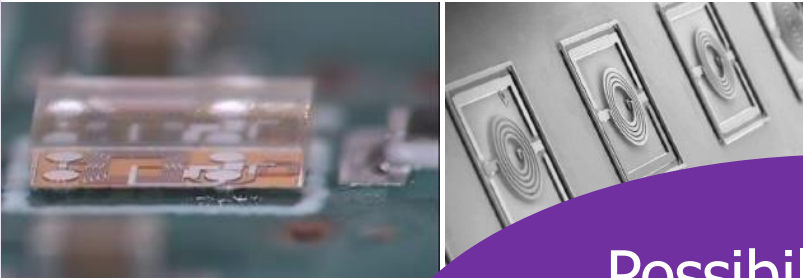


EDO KIRIKO  
[www.edokiriko.or.jp](http://www.edokiriko.or.jp)



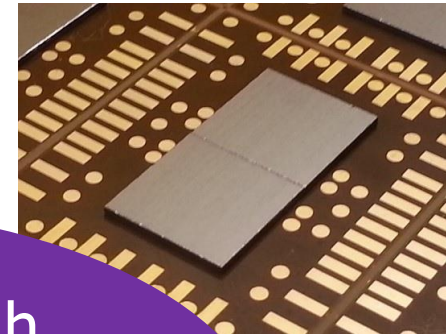
# Glass Benefit for Semiconductor Packaging

High Resistivity and Electrically Low Insertion Loss



Glass Passive Device  
Source: STmicroelectronics

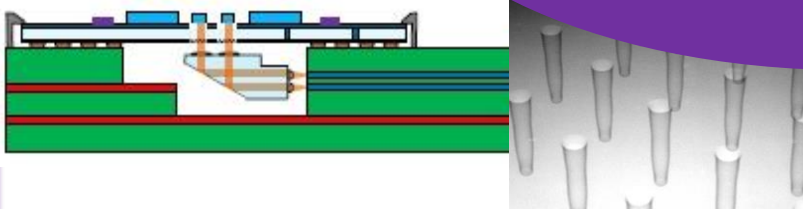
Dimensional Stability



Demonstrator  
Tech

Possibility of high volume and low cost based on panel size manufacturing

Transparency



Transceiver using TGV (Through Glass Vias)  
Source: Fraunhofer IZM, GIT2015



FOPLP using Glass Carrier  
Source: Sangyo Times

# Transition to Panel Level Manufacturing

Keyword

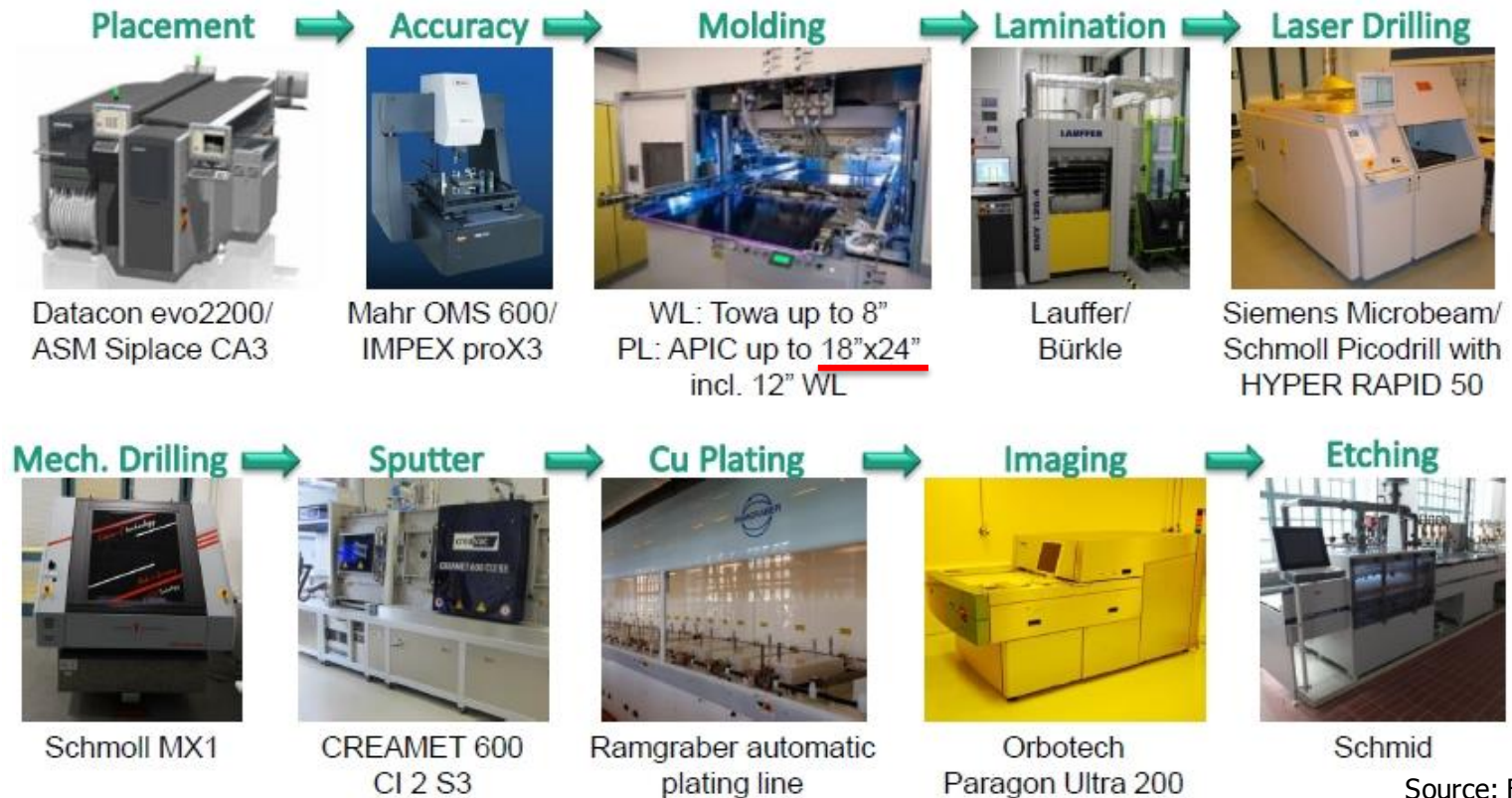
FOWL/FOPL

TGV

# FOWLP/PLP R&D activities around the world

## Fraunhofer IZM's PLP Consortium

Manufacturing line to transfer PLP technology to industry  
Focusing on Mold first approach



Source: Fraunhofer IZM



# FOWLP/PLP R&D activities around the world

## A\*STAR IME's FOPLP Consortium

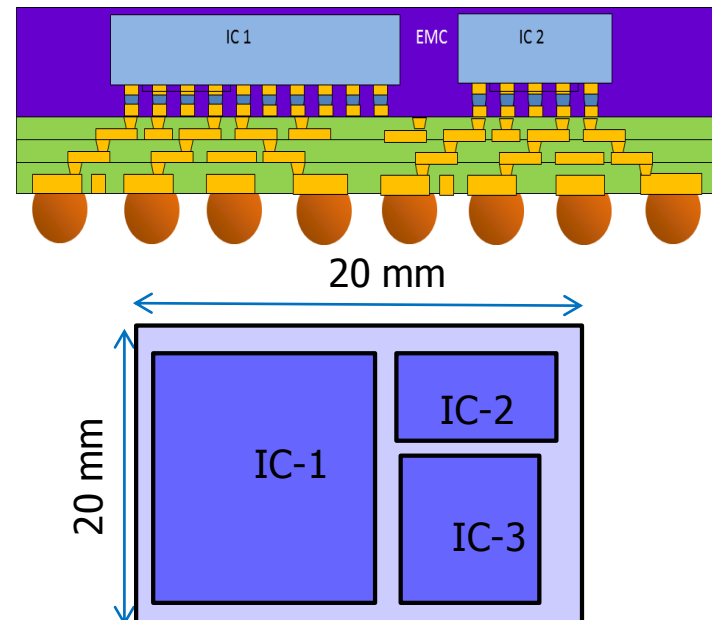
Focusing on RDL first approach

Plan to establish complete panel line by 2017



- Development of complete packaging process flow with Gen-3 panel
- Qualifying tools and materials for panel-base Fan-out multi-chip packaging

Package Specifications for Phase-1	
Target App	Tablet, smart phones
Package	20mm x20mm
Package thickness	450um
# of I/O	2400
# of chips/Pkg	3
Panel size	<u>550 mm x 650 mm</u>
RDL L/S	2 layers, (10/10, 5/5 um)
Benefits	Higher throughput → lower cost
Challenges	Handling large panel
Reliability	MSL3, TCOB 1000 cycles



Note: \* Spec to be finalized with consortium members

Source: A\*STAR IME, Modified by AGC

# Glass Carrier for FOWLP/PLP Manufacturing

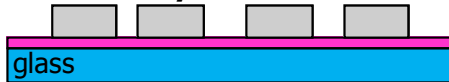
## Mold first

- Carrier for assembly and molding
- Temporary carrier for RDL processing (thin wafer handling, warpage compensation)

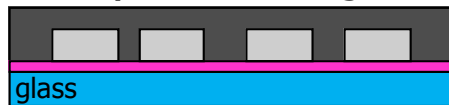
Apply thermal release tape on carrier



Die assembly on carrier



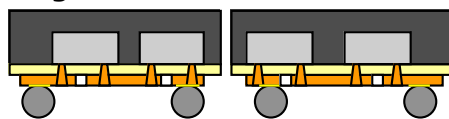
Wafer/panel overmolding



Carrier release



RDL (e.g. thin film, PCB based, ...), balling, singulation



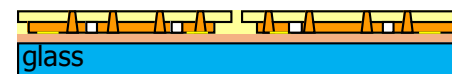
## RDL first

- Carrier for RDL build-up, assembly and molding

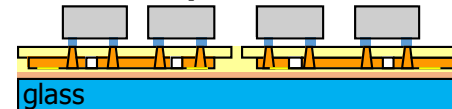
Apply release layer on carrier



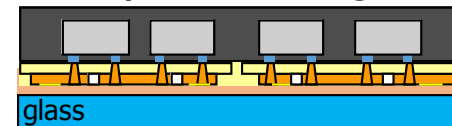
RDL (e.g. thin film, PCB based, ...)



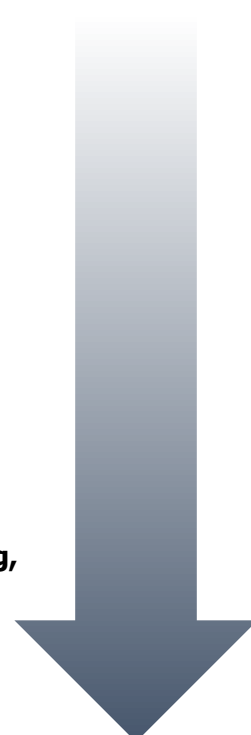
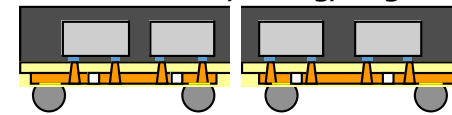
Die assembly on carrier



Wafer/panel overmolding



Carrier release, balling, singulation



Source: Fraunhofer IZM, Modified by AGC

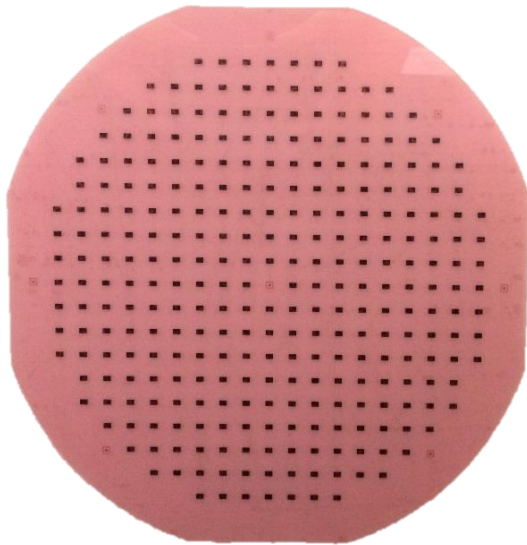
# Glass Lineup for FOWLP/FOPLP Carrier

	3~4 ppm/C	4~5 ppm/C	5~6 ppm/C	6~7 ppm/C	7~8 ppm/C	8~9 ppm/C	9~10 ppm/C	10~11 ppm/C	11~12 ppm/C
Alkali free	Available	Available	Available	Available	Available	Not Available	Not Available	Not Available	Not Available
Alkali	Not Available	Not Available	Not Available	Not Available	Available	Available	Available	Not Available	Available

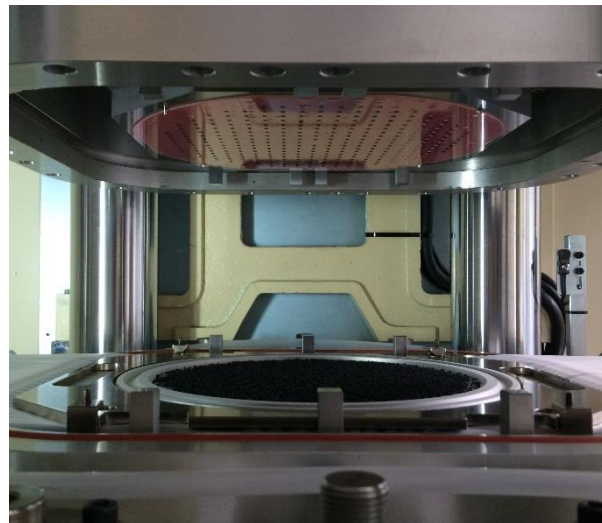
## Representative specification for 300mm glass carrier wafer

	Specification	Note
TTV	$\leq 5\mu\text{m}$	High spec : $\leq 1\mu\text{m}$
Ra	$\leq 1.5\text{nm}$	High spec : $\leq 0.5\text{nm}$
Warpage	$\leq 100\mu\text{m}$	High spec : $\leq 50\mu\text{m}$

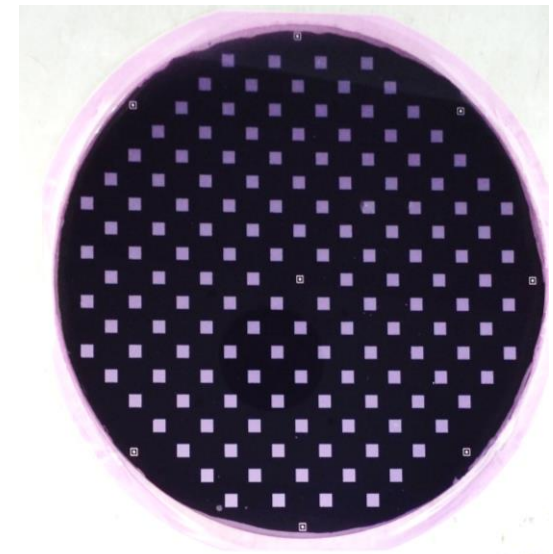
# FOWLP Assembly & Molding with Glass Carrier



Assembled glass carrier with thermo-release tape



Compression molding of assembled glass carrier

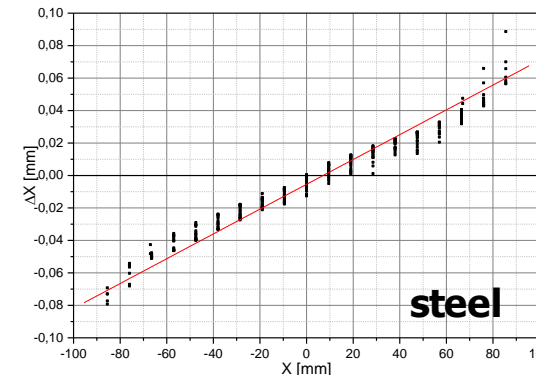
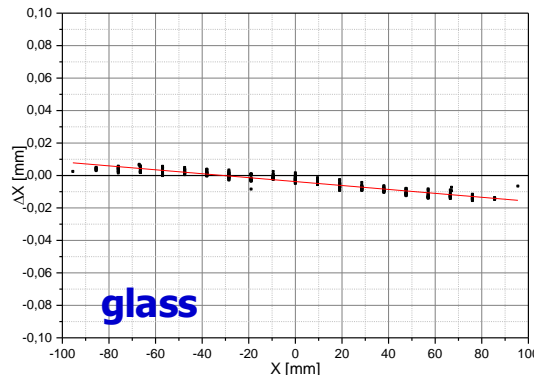


Molded glass carrier before carrier release

Source: Fraunhofer IZM ,Modified by AGC

# Die Shift Test Result

Die Shift Factor Comparison on Wafer between **Glass** (6,8 ppm/K by **AGC**) and Steel (12 ppm/K)



Carrier	X – Direction [mm/mm]	standard error	Y – Direction [mm/mm]	standard error
steel	$8,04 * 10^{-04}$	$0,261 * 10^{-04}$	$7,20 * 10^{-04}$	$0,200 * 10^{-04}$
glass	$0,87 * 10^{-04}$	$0,213 * 10^{-04}$	$0,65 * 10^{-04}$	$0,167 * 10^{-04}$

## Die Shift Factor:

Linear displacement of dies after molding (CTE EMC =  $\sim 8$  ppm/K)

-> mainly due to CTE mismatch and chemical shrinkage of EMC.

⇒ Die shift on the glass carrier is much lower than on the steel carrier.

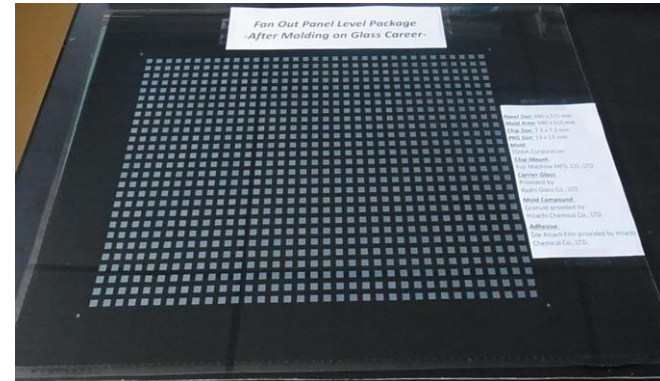
## Challenge: Robustness of glass carriers

Source: Fraunhofer IZM ,Modified by AGC

## FOPLP Warpage Test Results

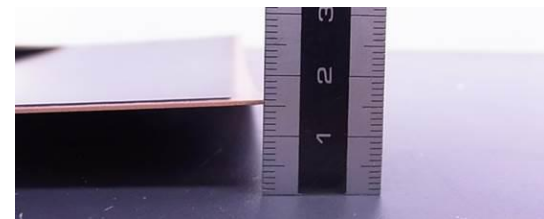
Panel size : 660 x 515 mm x 1 mmt  
 Die size : 7.3 x 7.3 mm (945 pieces)  
 Mold area : 640 x 495 mm x 0.4 mmt

- Die Mount @ Fuji Machine Mfg.
- Compression mold @ TOWA
- Carrier : Glass (AGC)
- Organic substrate (Hitachi Chemical)



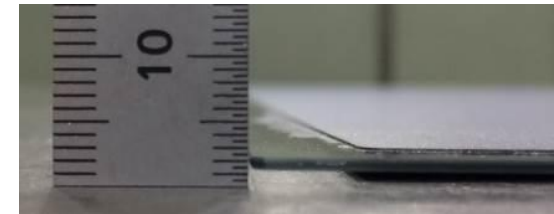
### Warpage: 15mm

EMC: Film type (CTE: 8 ppm/C)  
 Carrier: Organic substrate (CTE: 6 ppm/C)



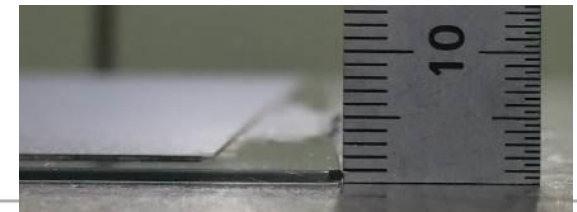
### Warpage: 3.0mm

EMC: Film type (CTE: 7 ppm/C)  
 Carrier: Glass (CTE: 9.6 ppm/C)

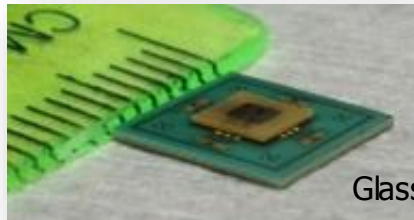


### Warpage: -1.35mm

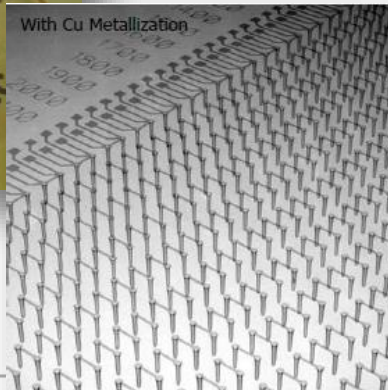
EMC: Granule type (CTE: 7 ppm/C)  
 Carrier: Glass (CTE: 8.3 ppm/C)



# Lab to Fab, TGV is getting to launch



Glass IPD

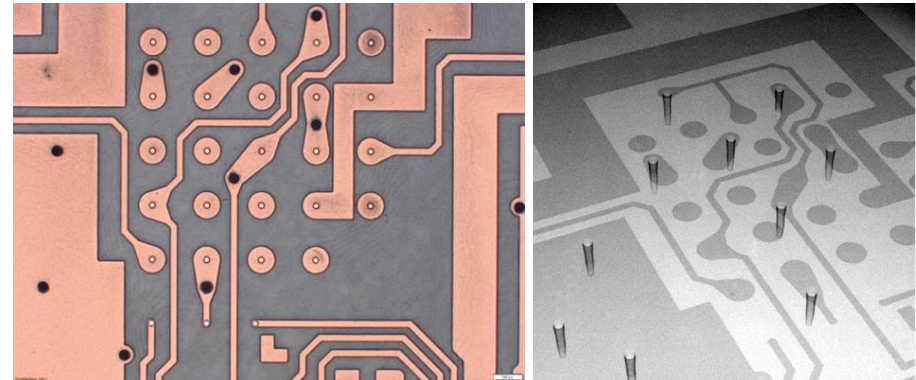


$\Phi 20\mu\text{m}$  TGV metallization by industrial partners



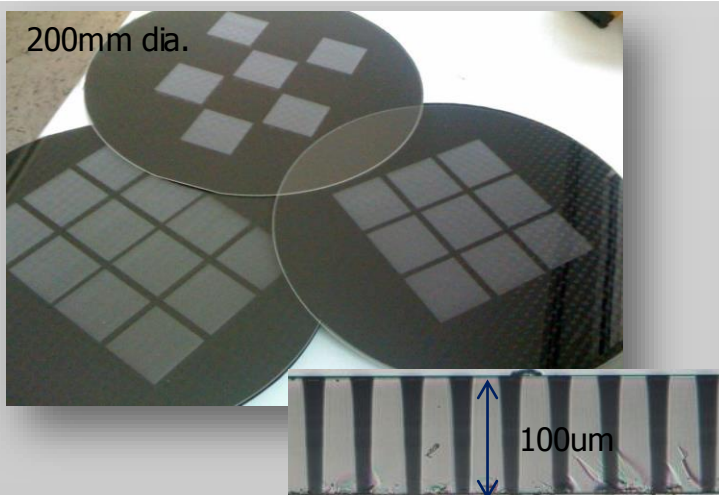
Source: Tango Systems

RF application

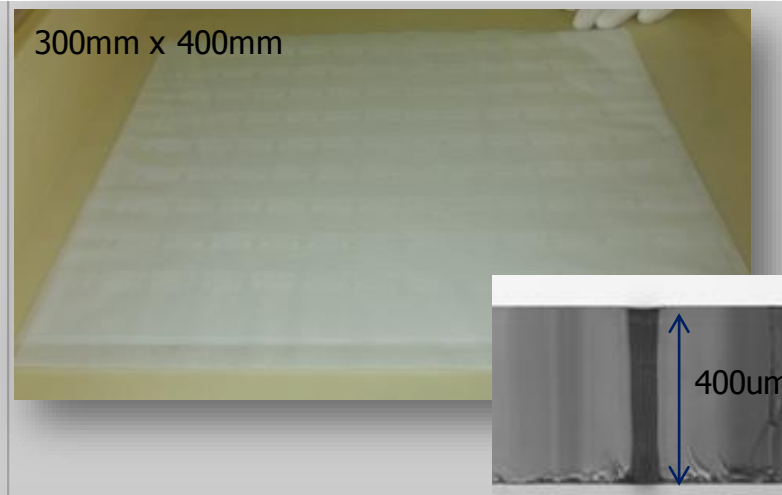


# TGV is moving to panel size

## Wafer



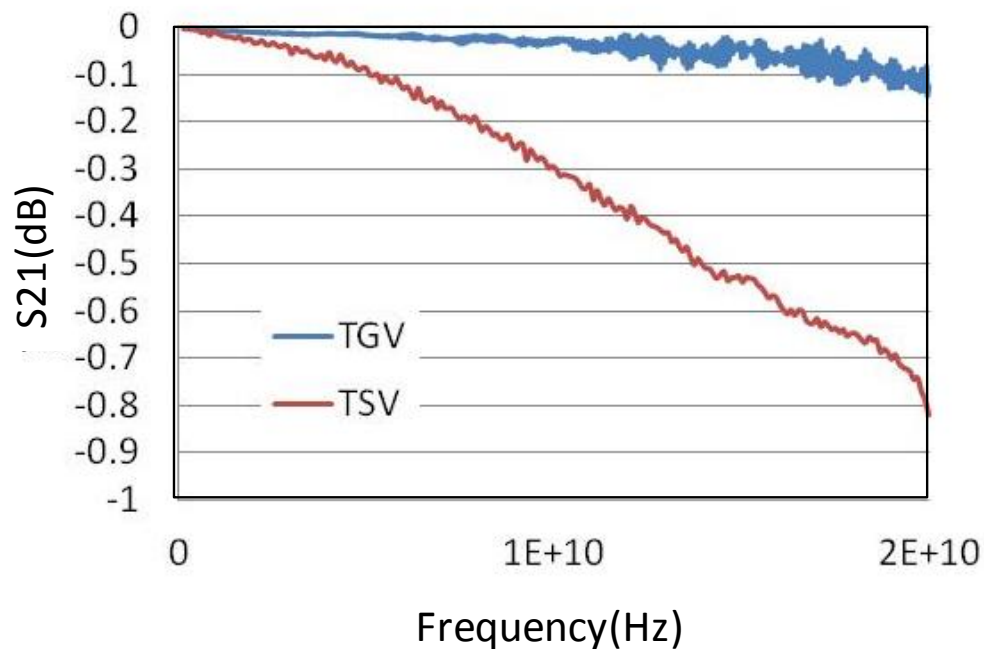
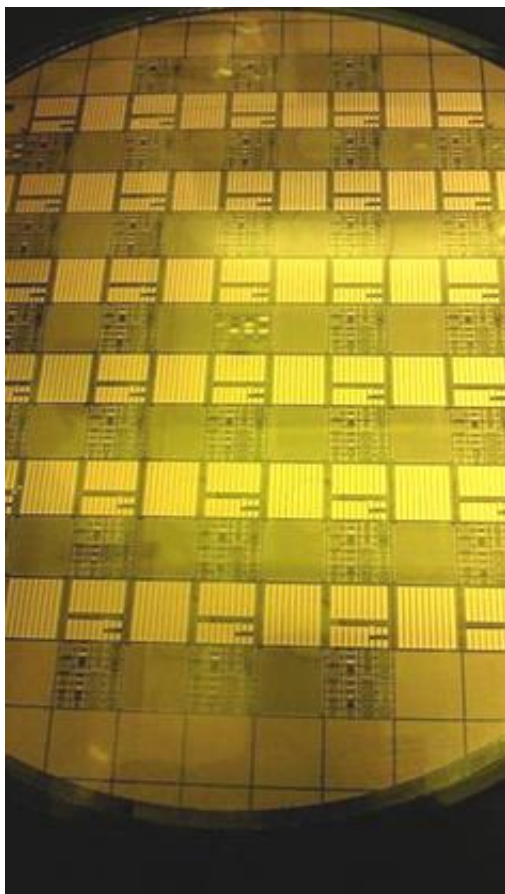
## Panel



Size	6inch, 8inch, 12inch	~550mm x 650mm (Gen-3)
Thickness	100~500um	100~500um
Representative Hole Size	$\phi 20 \sim 150 \mu\text{m}$	$\phi 65 \sim 150 \mu\text{m}$
Hole Pitch	Minimum 2x Hole Diameter	Minimum 2x Hole Diameter
TGV Metallization	Cu conformal plating, Cu full-filled plating, and Cu paste filling	Cu conformal plating



# TGV contributes to miniaturized RF devices

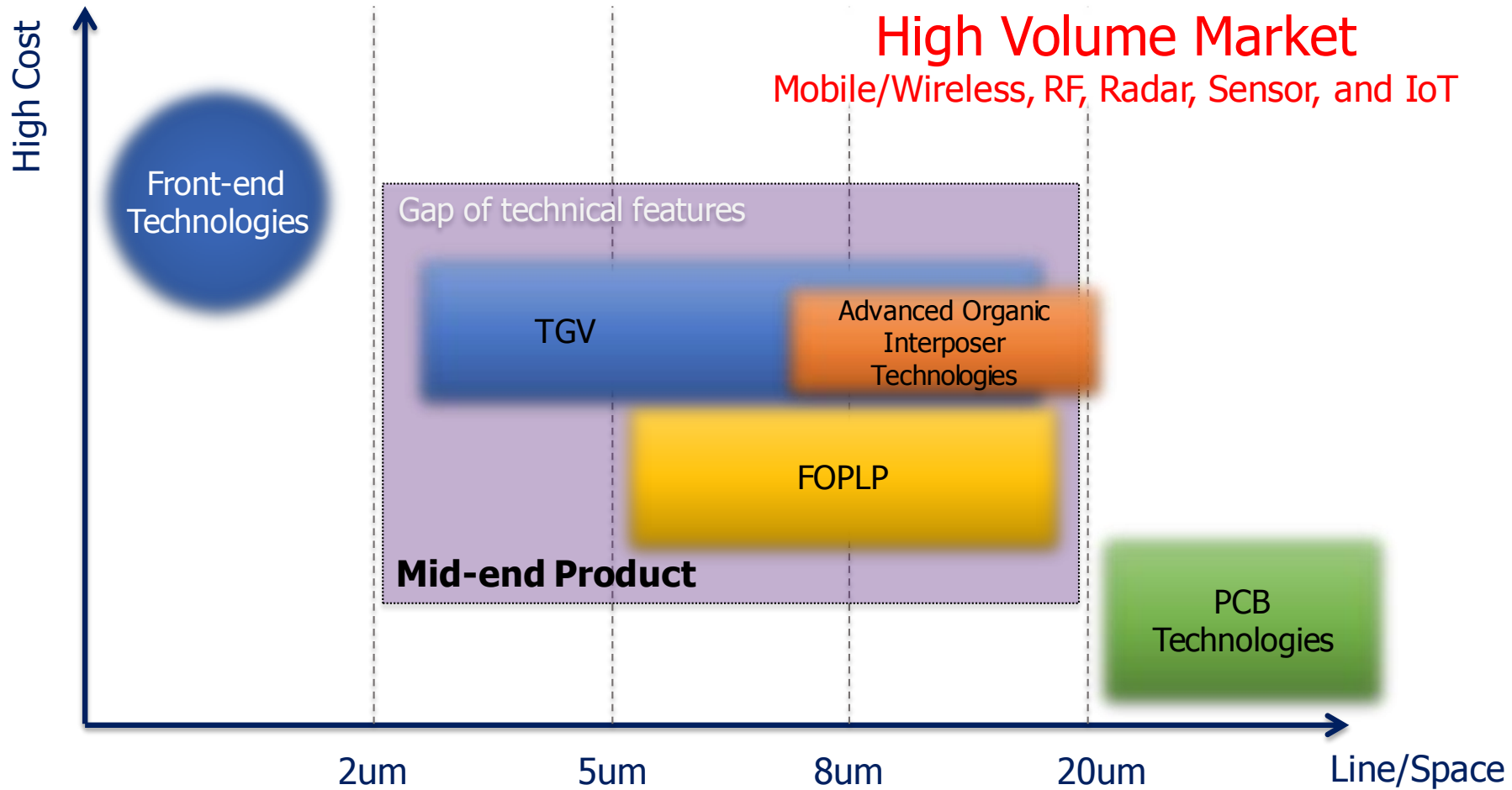


Highly bulk resistance of TGV resulted in insertion loss less than -0.12dB at 20GHz.

Source: Dai Nippon Printing

# Where Panel Technologies go

# The necessity of panel technologies



# Summary

- R&D consortium for FOPLP using large glass carrier is taking off. Glass panel is a good candidate as carrier material because of flat surface and an availability of different CTE.
- TGV is moving to panel size up to Gen-3 from wafer size. RF is a possible application based on better material properties (low insertion loss) of glass.
- Panel technologies will be an important to realize high volume manufacturing for mid-end products in a future connected world.

***“Look Beyond”***

Glass is only the Beginning.

**AGC**